

In the Claims

1. A memory system comprising:
  - 5 at least one memory device, with each of memory device comprising
    - (a) an array of memory cells;
    - (b) addressing circuitry adapted to address the memory cells;
    - (c) a bus interface;
    - (d) a command decoder which decodes commands at the bus interface, including an address assign command; and
    - (e) local address storage circuitry which stores a local address for the associated memory device once the address assign command is decoded by the command decoder; and
  - 10 a memory controller having a bus interface coupled to the bus interface of the memory device, with the memory controller providing the local address to be stored in the local address storage circuitry of the memory device of the memory system together with the address assign command.
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- 25 2. The memory system of Claim 1 wherein the bus interface of the memory controller is coupled to the bus interface of the memory device by a system bus.
- 30 3. The memory system of Claim 2 including a plurality of the memory devices wherein the memory controller transfers the local address to the memory

devices over the system bus and the address assign command over the system bus.

4. The memory system of Claim 3 wherein the memory controller has a select signal output and each of the memory devices has a select signal input and a select signal output, with the select signal output of the memory controller being coupled to the select signal input of a first one of the memory devices by a first select signal line and wherein the select signal output of the first memory device is coupled to the select signal input of a second one of the memory devices by a second select signal line.

5. The memory system of Claim 4 wherein the local address is transferred from the memory controller to the first one of the memory devices when the memory controller causes the select signal input of the first memory device to go active.

6. The memory system of Claim 5 wherein the local address is transferred from the memory controller to the second one of the memory devices when the first memory device causes the select signal input of the second memory device to go active.

7. The memory system of Claim 6 further including a third one of the memory devices wherein the local address is transferred from the memory controller to the third one of the memory devices when the second memory device causes the select signal input of the third memory device to go active.

8. The memory system of Claim 7 wherein the system bus includes a tag bus and a data bus, with the local address being transferred over the data bus.

5 9. The memory system of Claim 8 wherein each of the memory devices includes lockout circuitry switchable between a lockout state and a non-lockout state, with the select signal output of one of the memory devices being inactive when the lockout circuitry of the memory device is in the non-lockout state.

10 10. The memory system of Claim 9 wherein the select signal output of the memory device is active when both the select signal input of the memory device is active and the lockout circuitry of the memory device is in the lockout state.

15 11. The memory system of Claim 10 wherein transfer of the local address to the local address storage circuitry is blocked when the lockout circuitry is in the lockout state.

20 12. The memory system of Claim 11 further including reset circuitry which resets the local address storage circuitry subsequent to application of power to the local address storage circuitry.

25 13. The memory system of Claim 12 wherein the reset circuitry also resets the lockout circuitry to the non-lockout state subsequent to application of power to the lockout circuitry.

14. A memory system comprising:  
a system bus;

a memory controller coupled to the system bus;

a plurality of memory devices, with each of the memory devices including

5 (a) an array of memory cells;

(b) local address storage circuitry which stores a local address for the memory device, with the local address being provided by the memory controller;

10 (c) addressing circuitry adapted to address the memory cells;

(d) bus interface circuitry coupled to the system bus and which receives the memory device addresses for the addressing circuitry, with the interface circuitry switchable between an enabled mode and a disabled mode; and

15 (e) a select signal input and a select signal output, with the bus interface circuitry being in the enabled state when the select signal input is active.

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25 15. The memory system of Claim 14 wherein the memory controller has a select signal output, with the select signal output of the memory controller being coupled to the select signal input of a first one of the memory devices by a first select signal line and wherein the select signal output of the first memory device is coupled to the select signal input of a second one of the memory devices by a second select signal line and the select signal output of the second memory device is coupled to the select signal

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input of a third one of the memory devices by a third select signal line.

5           16. The memory system of Claim 15 wherein each of the memory devices includes lockout circuitry switchable between a lockout state and a non-lockout state, with the select signal output of the memory device being inactive when the lockout circuitry of that memory device is in the non-lockout state.

10           17. The memory system of Claim 16 wherein the select signal output of the memory devices is active when both the select signal input of the memory device is active and the lockout circuitry of the memory device is in the lockout state.

15           18. The memory system of Claim 17 wherein the memory devices are switchable between a device-enabled state where the device is capable of performing memory read operations and a device-disabled state where the memory device is not capable of performing memory read operations and wherein each memory device includes reset circuitry which resets the lockout circuitry to the non-lockout state subsequent to application of power to the lockout circuitry and wherein the memory devices are in the device-enabled state when both the select signal input is active and the lockout circuitry is in the non-lockout state.

20           25           19. The memory system of Claim 18 wherein the memory devices each include device select circuitry switchable between a device-selected state and a device-not-selected state, with the memory device being in the device-enabled state if both the device

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select circuitry is in the device-selected state and the lockout circuitry is in the lockout state.

5           20. The memory system of Claim 19 wherein the reset circuitry resets the device select circuitry to the device-not-selected state subsequent to application of power to the device select circuitry.

10           21. The memory system of Claim 20 wherein each memory device includes a comparator circuit which compares an address present on the system bus with the local address stored in the local address storage circuitry and wherein the device select circuitry can be switched to the device-selected state when there is a match between the address on the system bus and the local address.

15           22. The memory system of Claim 21 wherein each of the memory devices includes a command decoder configured to decode commands on the system bus, including select commands, and wherein the device select circuitry can be switched to the device-selected state when there are both a match between the address on the system bus and the local address, as determined by the comparator, and there is one of the select commands on the system bus, as determined by the command decoder.

20           23. The memory system of Claim 22 wherein the command decoder is configured to decode de-select commands and wherein the device select circuitry can be switched to the device-not-selected state when there are both a match between the address on the system bus and the local address, as determined by the comparator, and there is one of the deselect

commands on the system bus, as determined by the command decoder.

24. The memory system of Claim 23 wherein the system bus includes a tag bus and a data bus, with the tag bus being coupled to the command decoder of the memory devices and with the data bus being coupled to the comparator.

25. A memory system comprising:  
10 a system bus which includes a tag bus and a data bus;

15 a memory controller coupled to the system bus;

20 a plurality of memory devices, with each of the memory devices including

25 (a) an array of memory cells;

30 (b) local address storage circuitry coupled to the data bus which stores a local address for the memory device originating from the memory controller;

(c) a comparator coupled to the data bus which compares an address on the data bus originating from the memory controller with the local address stored in the local address circuitry; and

35 (d) a command decoder coupled to the tag bus which decodes commands originating from the memory controller, including commands to perform memory read operations on the memory device.

40 26. The memory system of Claim 25 wherein the memory devices each include a select signal input and a select signal output and a lockout circuit switchable

between a lockout state and a non-lockout state and wherein the select signal output is active provided both the select signal input is active and the lockout circuit is in the lockout state.

5        27. The memory system of Claim 26 wherein the memory devices are switchable between a device-enabled state where the memory device is capable of performing memory read operations and a device-disabled state where the memory device is not capable of performing memory read operations and wherein the memory devices are in the device-enabled state when both the select signal input is active and the lockout circuitry is in the non-lockout state.

10        28. The memory system of Claim 27 wherein the memory devices include interface circuitry coupled to the system bus, with the interface circuitry being switchable between an enabled state and a disabled state, with the interface circuitry being in the enabled state when the select signal input is active.

15        29. The memory system of Claim 28 wherein the local address comprises at least three bits and the local address is transferred over the data bus to the local address storage circuitry in parallel.

20        30. The memory system of Claim 29 wherein lockout circuitry is switchable to the lockout state only when the command decoder decodes a select command.

25        31. The memory system of Claim 30 wherein the memory devices include reset circuitry for resetting the lockout circuitry to the non-lockout state subsequent to application of power to the lockout circuitry.

32. The memory system of Claim 31 wherein transfer of the local address from the data bus to the local address storage circuitry is blocked when the lockout circuitry is in the lockout state.

5 33. The memory system of Claim 32 wherein memory read operations on the memory devices are carried out by transferring an address for the memory device to be read over the data bus.

10 34. The memory system of Claim 33 wherein the memory read operations on the memory devices are carried out by transferring the data read from the memory devices over the data bus.

15 35. The memory system of Claim 34 wherein the memory controller includes a select signal output and the system includes first, second and third memory devices, with the select signal output of the memory controller being coupled to the select signal input of the first memory device by way of a first select line, with the select signal output of the first memory device being coupled to the select signal input of the second memory device by way of a second select line and with the select signal output of the second memory device being coupled to the select signal input of the third memory device.

20 36. A memory device for use in a memory system which includes a memory controller and a plurality of the memory devices, with the memory controller and memory devices being coupled to a common system bus, the memory devices including:

25 an array of memory cells;

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a command decoder which detects a select commands on system bus;

a lockout circuit switchable from non-lockout state to a lockout state when one of the select commands is detected;

a select signal input and a select signal output;

local address storage circuitry which stores a local address for the memory device provided by the memory controller over the data bus; and

a blocking circuit which prevents transfer of the local address from the system bus to the local address storage circuitry unless the lockout circuit is in the non-lockout state.

37. The memory device of Claim 36 wherein the select signal output is active if both the select signal input is active and the lockout circuitry is in the lockout state.

38. The memory device of Claim 37 wherein the system bus includes a data bus and a tag bus and wherein the command decoder is coupled to the tag bus and the local address is received on the data bus.

39. The memory device of Claim 38 wherein the command decoder detects memory read commands on the tag bus which causes the memory device to read data stored in the memory device at an address provided by the memory controller over the data bus.

40. A method of controlling the operation of a memory system which includes a plurality of memory devices, each memory device including an array of

memory cells and coupled to a common system bus, the method comprising the following steps:

causing a select input of a first one of the memory devices to become active;

5 placing an address assign command on the system bus;

transferring a first local address over the system bus to the first one of the memory devices;

10 storing the first local address in the first memory device;

causing a select output of the first memory device to become active in response to receipt of the address assign command by the first one of the memory devices;

15 forwarding the active select output of the first memory device to a select input of a second one of the memory devices;

20 placing an address assign command on the system bus;

transferring a second local address over the system bus to the second memory device;

25 storing the second local address in the second memory device;

causing a select output of the second memory device to become active in response to receipt of the address assign command by the second one of the memory devices;

30 forwarding the active select output of the second memory device to a select input of a third one of the memory devices;

placing an address assign command on the system bus; and

35 transferring a third local address over the system bus to the third memory device; and

storing the third local address in the third memory device.

5 41. The method of Claim 40 wherein the steps of storing the first, second and third local addresses each include the step of testing whether a lockout circuit is in a lockout state or a non-lockout state.

10 42. The method of Claim 41 wherein the steps of causing the select outputs to become active include the steps of testing whether the lockout circuit is in the lockout or non-lockout state.

15 43. The method of Claim 42 wherein the system bus includes a tag bus and a data bus and wherein the first, second and third local addresses are transferred over the data bus and wherein the address assign commands are placed on the tag bus.

20 44. The method of Claim 43 further including the step of performing a read operation on a selected one of the three memory devices by placing an address on the data bus that corresponds to the local address stored in the selected memory device and by placing the data read from the selected memory device on the data bus.

25 45. The method of Claim 44 wherein the step of performing the read operation further includes the step of placing a read command on the tag bus.

46. The method of Claim 40 further including the step of placing a select command on the system bus, with the select command containing one of the local

addresses and switching the memory device to a device-enabled state in response to receipt of the select command by the memory device having a stored local address which corresponds to the local address contained in the select command and performing a read operation on the memory device in the device-enabled state.

47. A method of controlling the operation of a memory system that including a plurality of memory devices connected to a common system bus, with each of the memory devices including an array of memory cells and addressing circuitry which is used to address the array of memory cells, the method comprising the following steps:

transferring a first local address to the first memory device, with the first local address comprising at least three bits of address that are transferred to the first memory device over the system bus in parallel;

selecting a second one of the memory devices;

transferring a third local address to the third memory device, with the third local address comprising at least three bits of

address that are transferred to the third memory device over the system in parallel.

48. The method of Claim 47 wherein the memory devices each include a select input and a select output and wherein the step of selecting the first memory device includes the step of causing the select input to become active.

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49. The method of Claim 48 wherein the step of selecting the second memory device includes the steps of causing the select output of the first memory device to become active and forwarding the active select output of the first memory device to the select input of the second memory device.

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50. The method of Claim 49 wherein the step of selecting the third memory device includes the steps of causing the select output of the second memory device to become active and forwarding the active select output of the second memory device to the select input of the third memory device.

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51. The method of Claim 50 wherein steps of causing the select outputs of the first and second memory devices to go active includes the step of setting lockout circuitry in the first and second memory devices from a non-lockout state to a lockout state.

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52. The method of Claim 51 wherein the steps of setting the lockout circuitry to the lockout state each includes the step of placing an address assign command on the system bus.

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53. The method of Claim 52 wherein the system bus includes a tag bus and a data bus and wherein the address assign command is placed on the tag bus and wherein the local addresses are transferred to the memory devices by way of the data bus.

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54. The method of Claim 53 further including the step of performing memory read operations on a selected one of the memory devices after the local address is transferred to the selected memory device, with the step of performing the memory read operation including the steps of placing a memory read command on the tag bus and a memory read address on the data bus and the data read from the selected memory device on the data bus.

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55. The method of Claim 47 including the step of selecting one of the memory devices, subsequent to the step of transferring local addresses to the memory devices, by transferring a select command over the system bus containing an address that corresponds the local address transferred to the memory device to be selected, switching the memory device to be selected to a device-enabled state in response to receipt of the select command.

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56. The method of Claim 55 further including the step of performing a memory read operation on the memory device in the device-enabled state.

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57. The method of Claim 56 further including the step of switching the memory device in the device-enabled state to a device-disabled state by transferring a deselect command to the memory device to be switched, said deselect command containing an

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address which corresponds to the local address transferred to the memory device to be switched to the device-disabled state.

58. A memory system comprising:

5 a plurality of separate memory devices,  
with each of the memory devices comprising  
(a) an array of memory cells;  
(b) addressing circuitry adapted to  
address the memory cells;  
10 (c) a bus interface;  
(d) a command decoder which decodes  
commands at the bus interface,  
including an address assign command;  
and  
15 (e) local address storage circuitry  
which stores a local address for the  
associated memory device once the  
address assign command is decoded by  
the command decoder;  
20 (f) a lockout circuit switchable  
between a lockout state and a non-  
lockout state;  
(f) a select signal input and a  
select signal output, with the select  
signal output being active when both  
25 the select signal input is active and  
the lockout circuit is in the non-  
lockout state; and  
a memory controller having a bus interface  
30 coupled to the bus interface of each of the  
memory devices, with the memory controller  
having a select signal output connected to the  
select signal input of at least one of the  
memory devices.

59. The memory system of Claim 58 wherein the memory controller has a separate select signal output connected to the select signal input of each of the memory devices so that the memory controller can select one of the memory devices by causing the select signal output connected to the memory device to be selected to become active.

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60. The memory system of Claim 58 wherein the memory controller has a select signal output connected to the select signal input of a first one of the memory devices and wherein the select signal output of the first memory device is connected to the select signal input of a second one of the memory devices.

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61. The memory system of Claim 58 wherein the memory controller is configured to provide a plurality of separate select signal outputs and wherein the separate memory devices are arranged in a plurality of banks, with each bank comprising a plurality of the memory devices, with a first one of the memory devices of each of the banks having a separate select signal input connected to a separate one of the select signal outputs of the memory controller.

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62. The memory system of Claim 61 wherein a second one of the memory devices of each of the banks has the select signal input connected to the select signal output of the first memory device of the bank.

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63. The memory system of Claim 62 wherein a third one of the memory devices of each of the banks has the select signal input connected to the select signal output of the second memory device of the bank.

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